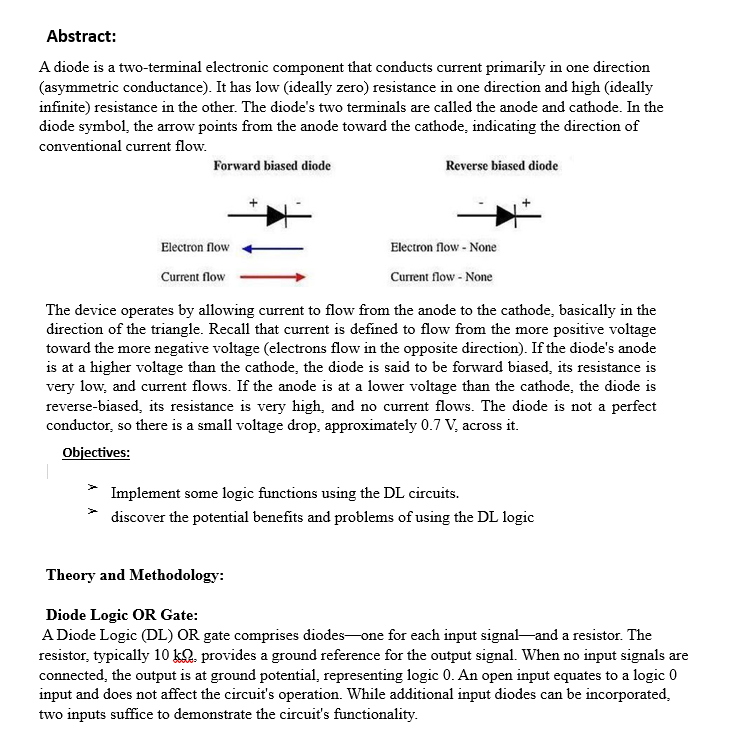
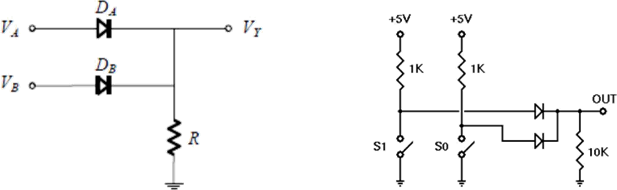
|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| AIUB | **American International University- Bangladesh (AIUB)**  **Faculty of Engineering (FE)** | | | | | | | | | |
|  | |  | | | | |  | |  | |
| **Course Name :** | | Digital Logic & Circuits Laboratory | | | | | **Course Code :** | | EEE 1204 | |
| **Semester :** | | Fall 2024-25 | | | | | **Sec :** | | G | |
| **Lab Instructor :** | | MD. ALOMGIR KABIR | | | | | **Group :** | | 07 | |
|  | |  | | | | |  | |  | |
| **Experiment No :** | | 05 | | | | | | | | |
| **Experiment Name :** | | Construction of Diode and Transistor Logic Gates | | | | | | | | |
|  | |  | | | | |  | |  | |
| **Submitted by (NAME):** | | **MOHAMMAD ANSAR UDDIN** | | | | **Student ID:** | | | **22-47975-2** | |
|  | |  | | | |  | | |  | |
| **Group Members** | | | | | **ID** | | | **Name** | | |
|  | | | | 1. | 22-48056-2 | | | CHINMOY GUHA | | |
|  | | | | 2. | 22-48067-2 | | | SUVRA CHAKRABORTY | | |
|  | | | | 3. | 22-47975-2 | | | MOHAMMAD ANSAR UDDIN | | |
|  | | | | 4. | 22-49393-3 | | | EFAZ MASHRUR AMIN | | |
|  | | | | 5. | 22-49385-3 | | | NAZMUL HASSAN NAYEEM | | |
|  | | | | 6. |  | | |  | | |
|  | | | | 7. |  | | |  | | |
|  | | | | |  | |  | |  | |
| **Performance Date :** | | | **20/11/24** | | | **Due Date :** | | | | **27/11/24** |
|  | | | | |  | | | | | |

**Marking Rubrics (to be filled by Lab Instructor)**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Category | Proficient  [6] | Good  [4] | Acceptable  [2] | Unacceptable [1] | Secured Marks |
| **Theoretical Background, Methods  & procedures sections** | All information, measures and variables are provided and explained. | All Information provided that is sufficient, but more explanation is needed. | Most information correct, but some information may be missing or inaccurate. | Much information missing and/or inaccurate. |  |
| **Results** | All of the criteria are met; results are described clearly and accurately; | Most criteria are met, but there may be some lack of clarity and/or incorrect information. | Experimental results don’t match exactly with the theoretical values and/or analysis is unclear. | Experimental results are missing or incorrect; |  |
| **Discussion** | Demonstrates thorough and sophisticated understanding. Conclusions drawn are appropriate for analyses; | Hypotheses are clearly stated, but some concluding statements not supported by data or data not well integrated. | Some hypotheses missing or misstated; conclusions not supported by data. | Conclusions don’t match hypotheses, not supported by data; no integration of data from different sources. |  |
| **General formatting** | Title page, placement of figures and figure captions, and other formatting issues all correct. | Minor errors in formatting. | Major errors and/or missing information. | Not proper style in text. |  |
| **Writing & organization** | Writing is strong and easy to understand; ideas are fully elaborated and connected; effective transitions between sentences; no typographic, spelling, or grammatical errors. | Writing is clear and easy to understand; ideas are connected; effective transitions between sentences; minor typographic, spelling, or grammatical errors. | Most of the required criteria are met, but some lack of clarity, typographic, spelling, or grammatical errors are present. | Very unclear, many errors. |  |
| Comments: |  | | | Total Marks  (Out of ): |  |





# Fig. 1 DL OR Gate

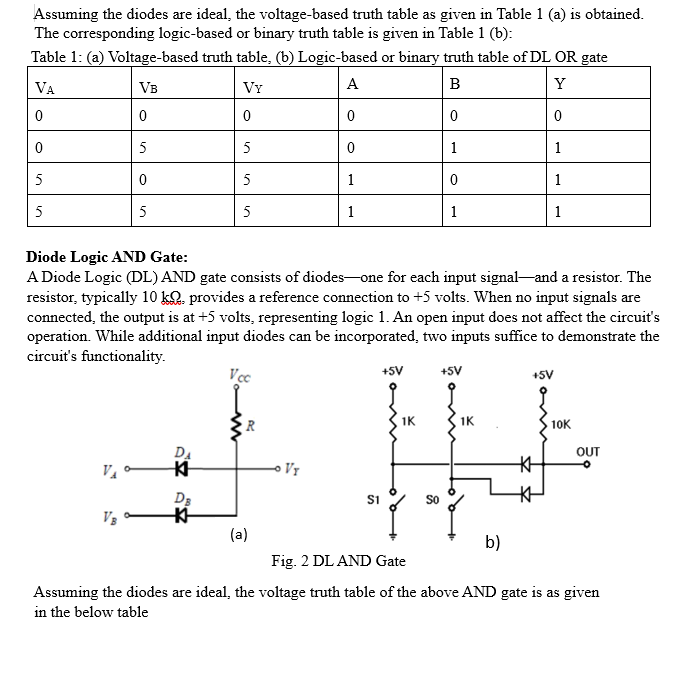
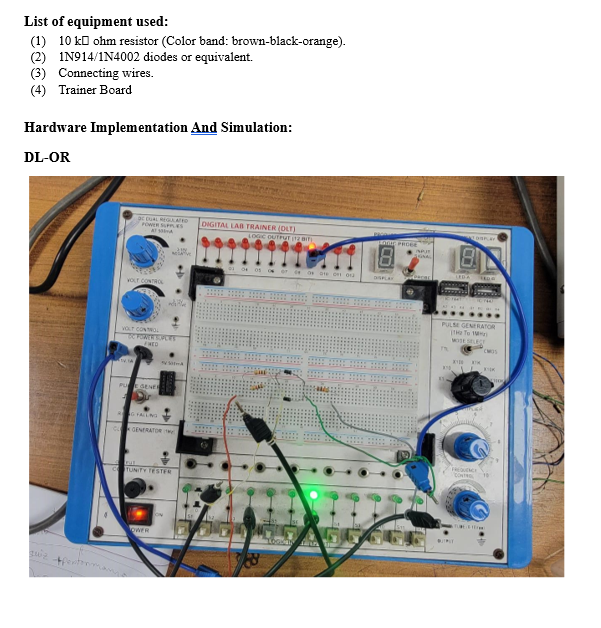


Table 2: (a) Voltage-based truth table, (b) Logic-based or binary truth table of DL AND gate Tab

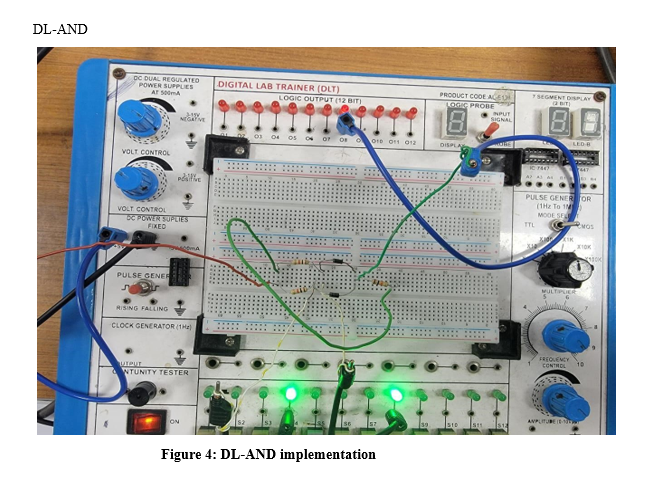
|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| VA | VB | VY | A | B | Y |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 5 | 0 | 0 | 1 | 0 |
| 5 | 0 | 0 | 1 | 0 | 0 |
| 5 | 5 | 5 | 1 | 1 | 1 |

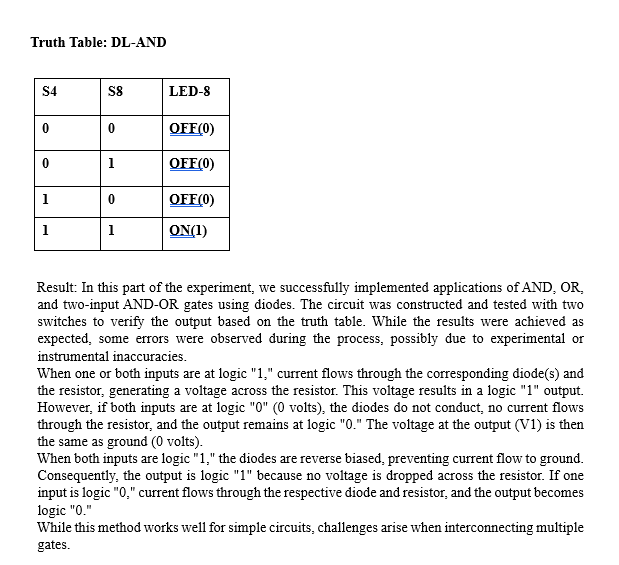


**Figure 3: DL-OR implementation**

**Truth Table: DL-OR**

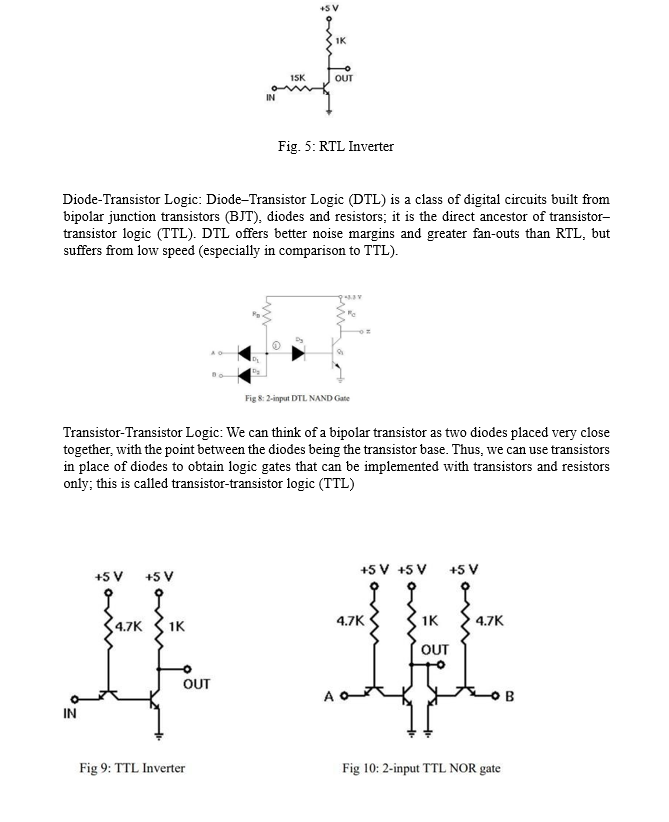
|  |  |  |
| --- | --- | --- |
| **S4** | **S7** | **LED-9** |
| **0** | **0** | **OFF(0)** |
| **0** | **1** | **ON(1)** |
| **1** | **0** | **ON(1)** |
| **1** | **1** | **ON(1)** |





**Part 2: Construction of Bipolar Transistor Logic Gate:**

Resistor-Transistor Logic (RTL): Resistor-Transistor Logic (RTL) represents a significant improvement over Diode Logic (DL) by replacing the diode switch with a transistor switch. When a +5V signal (logic "1") is applied to the base of the transistor through a resistor (used to limit the base-emitter voltage and current), the transistor turns fully on, grounding the output signal. If the input is at ground (logic "0"), the transistor remains off, allowing the output signal to rise to +5V.



**Emitter-Coupled Logic (ECL):**

In Emitter-Coupled Logic (ECL), when a HIGH input is applied to any of the circuit's inputs, the corresponding transistors turn ON, causing the output voltage (Vo) to drop to a LOW level. Conversely, when a LOW input is applied to all the transistors, they remain OFF. This allows the output (Vo) to rise to a HIGH level due to the voltage drop across the 640 Ω resistor.

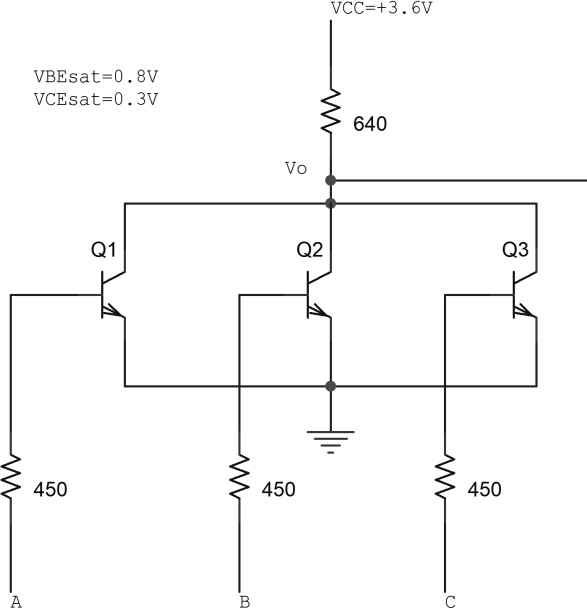


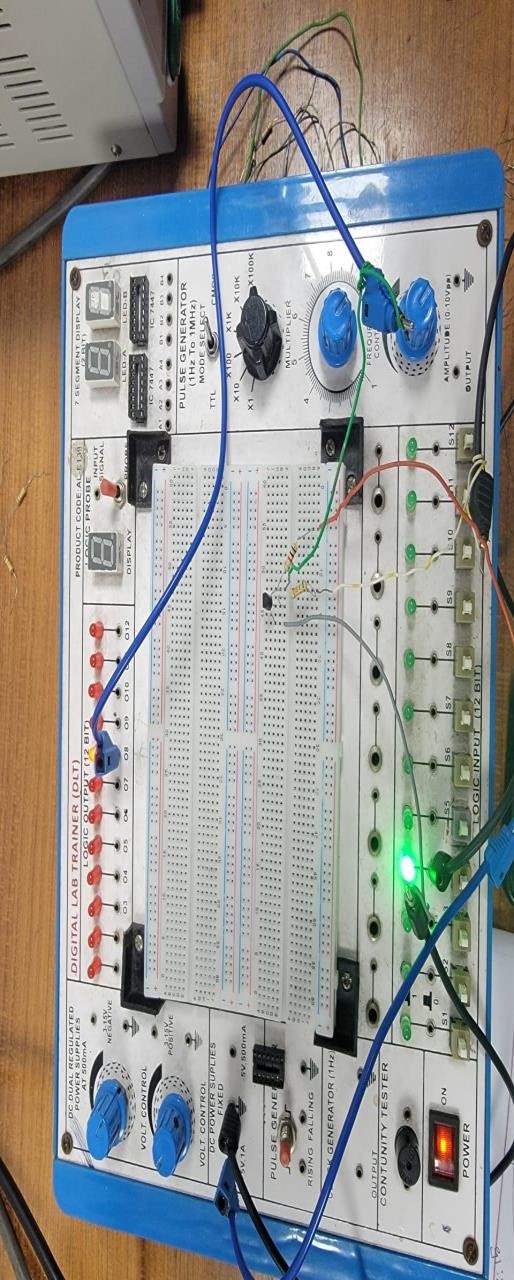
Fig. 6 A 3-input ECL NOR gate

**List of equipment used:**

* 2N4124 NPN silicon transistor (or equivalent).
* Resistors 15KΩ, 1KΩ, 4.7 KΩ
* Connecting wires.
* Trainer Board

**Hardware Implementation and Simulation:**

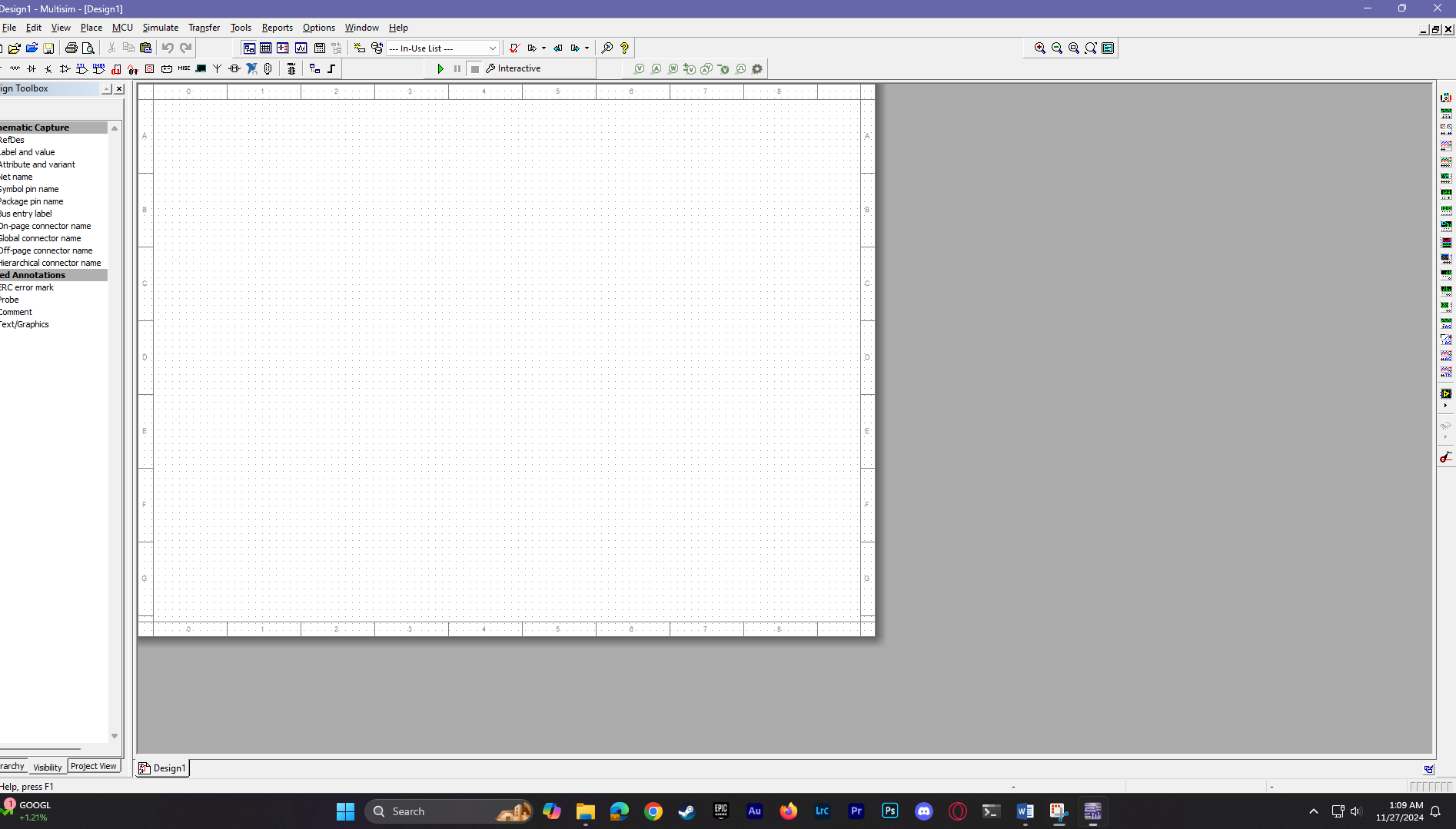
**RTL Inverter**

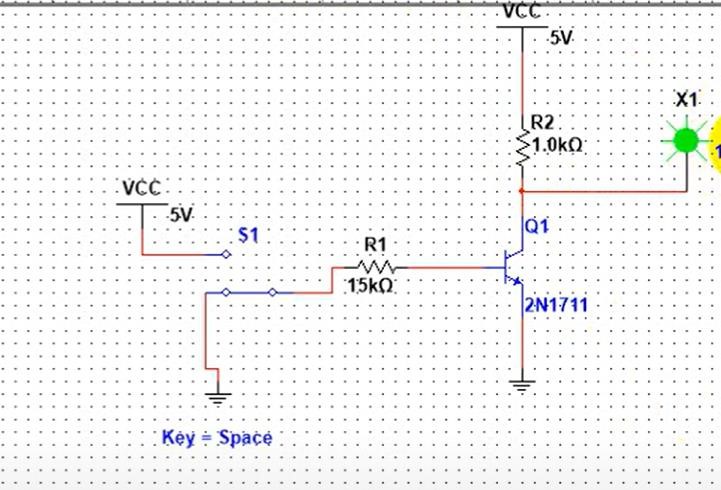


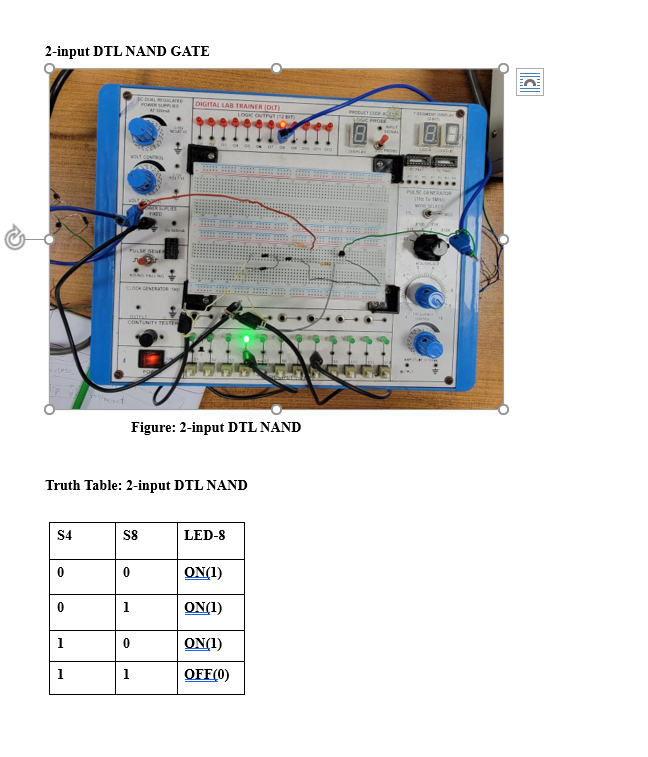
**Truth Table: RTL Inverter**

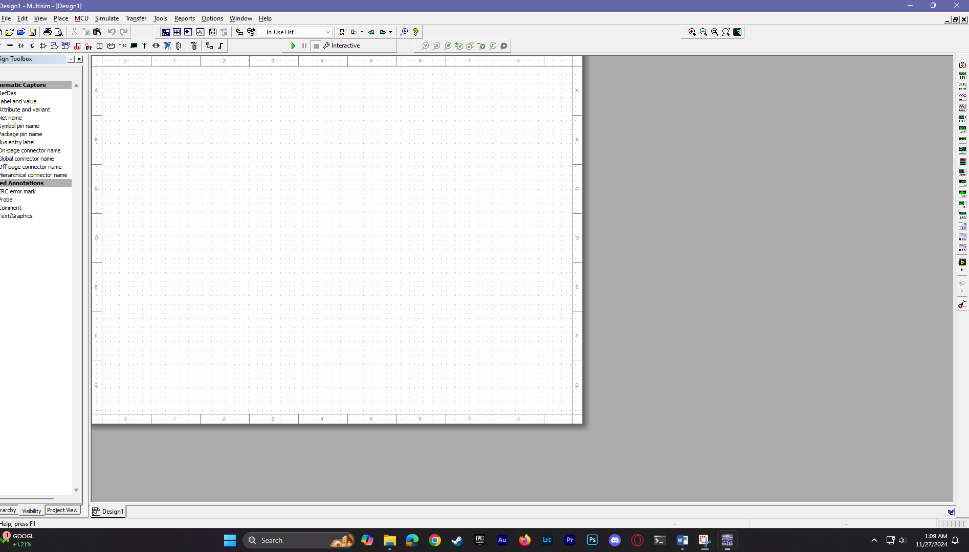
|  |  |
| --- | --- |
| **S4** | **LED** |
| **0** | **ON(1)** |
| **1** | **OFF(0)** |

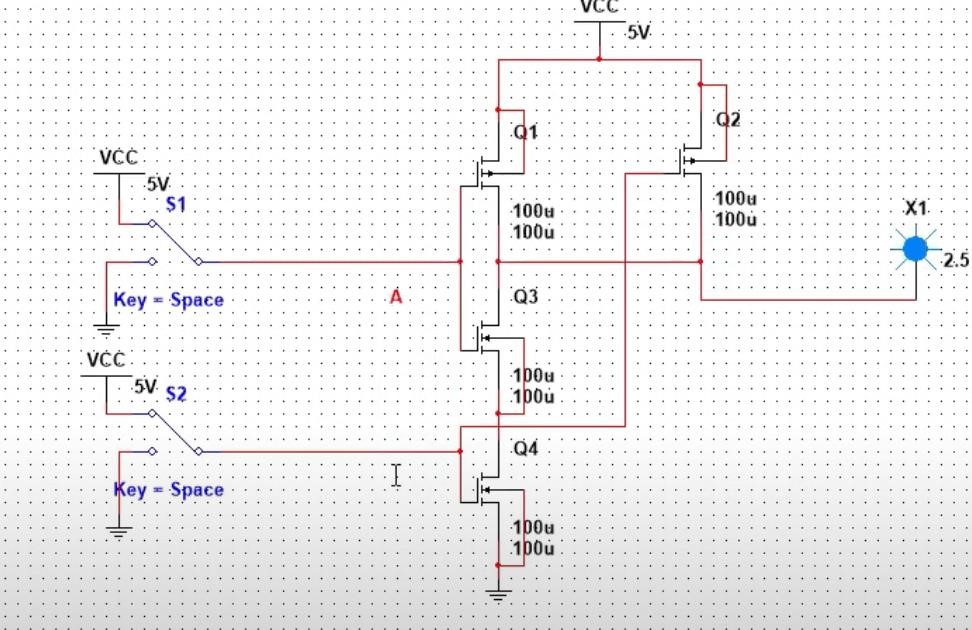
**Simulation :**



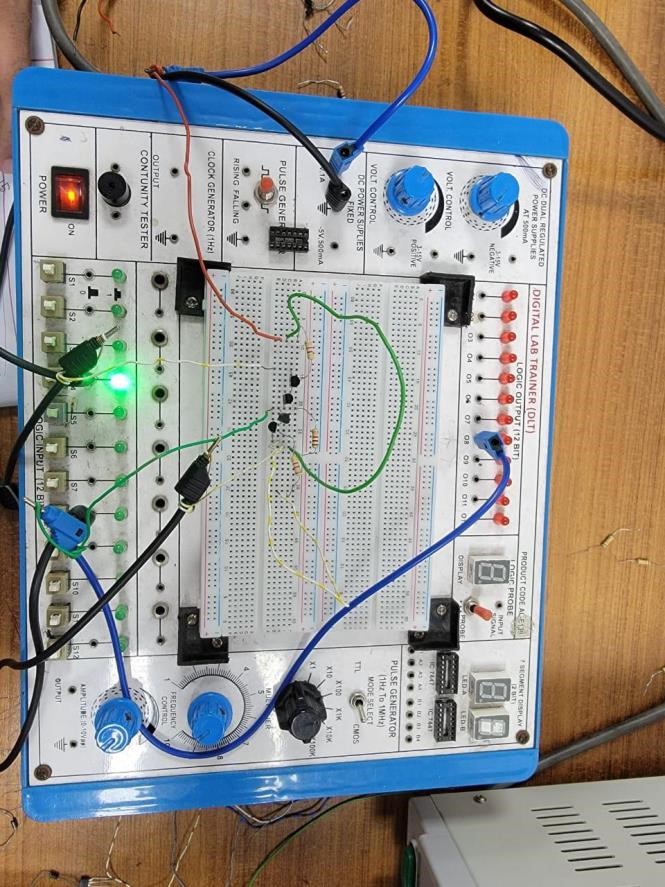


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**Simulation: 2-input DTL NAND**



**2-input TTL NOR GATE:**

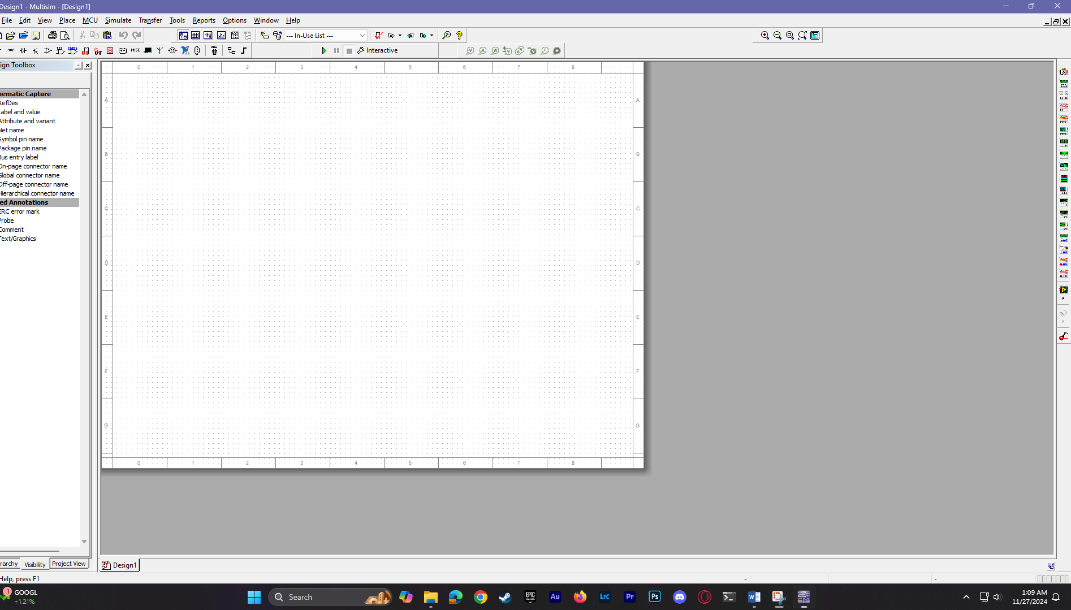


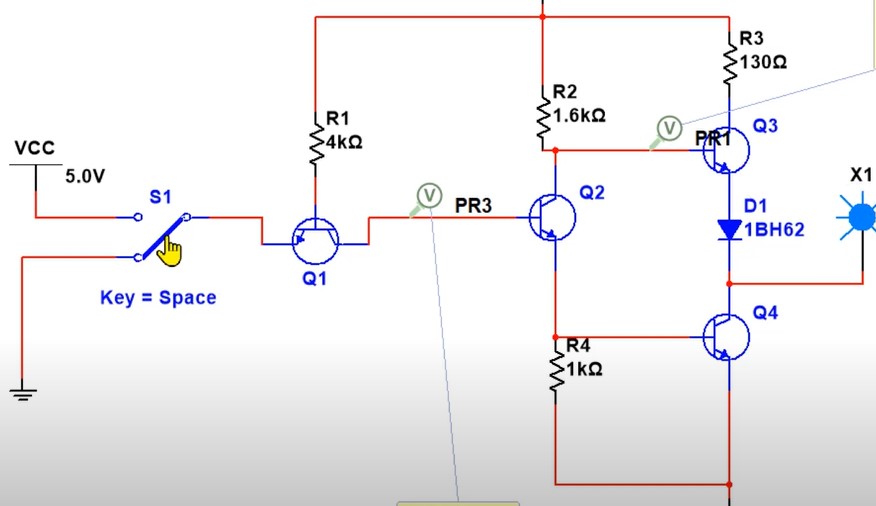
**Figure:2-input TTL NOR**

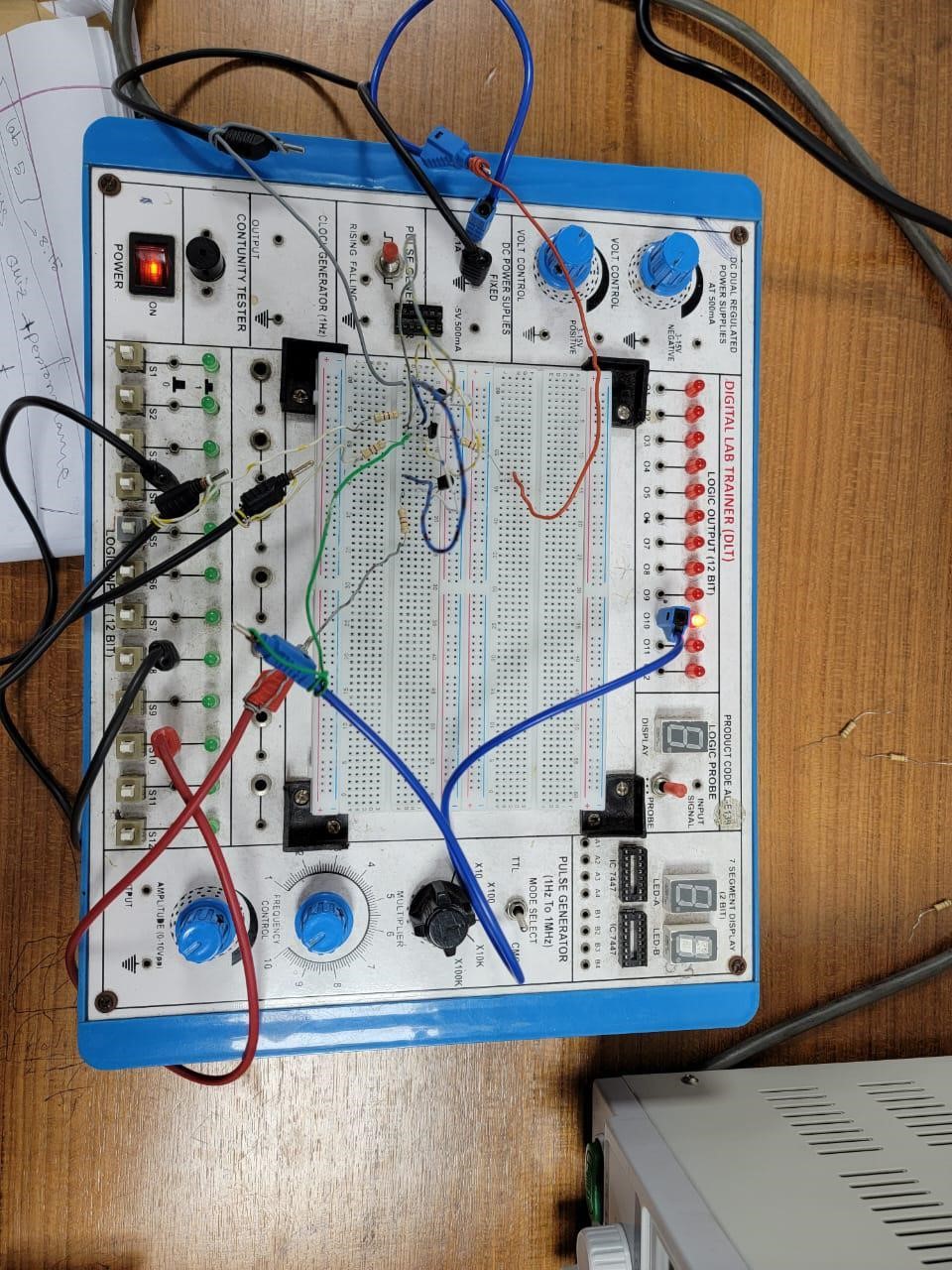
**Truth Table:2-input TTL NOR**

|  |  |  |
| --- | --- | --- |
| **S4** | **S8** | **LED-10** |
| **0** | **0** | **ON(1)** |
| **0** | **1** | **OFF(0)** |
| **1** | **0** | **OFF(0)** |
| **1** | **1** | **OFF(0)** |

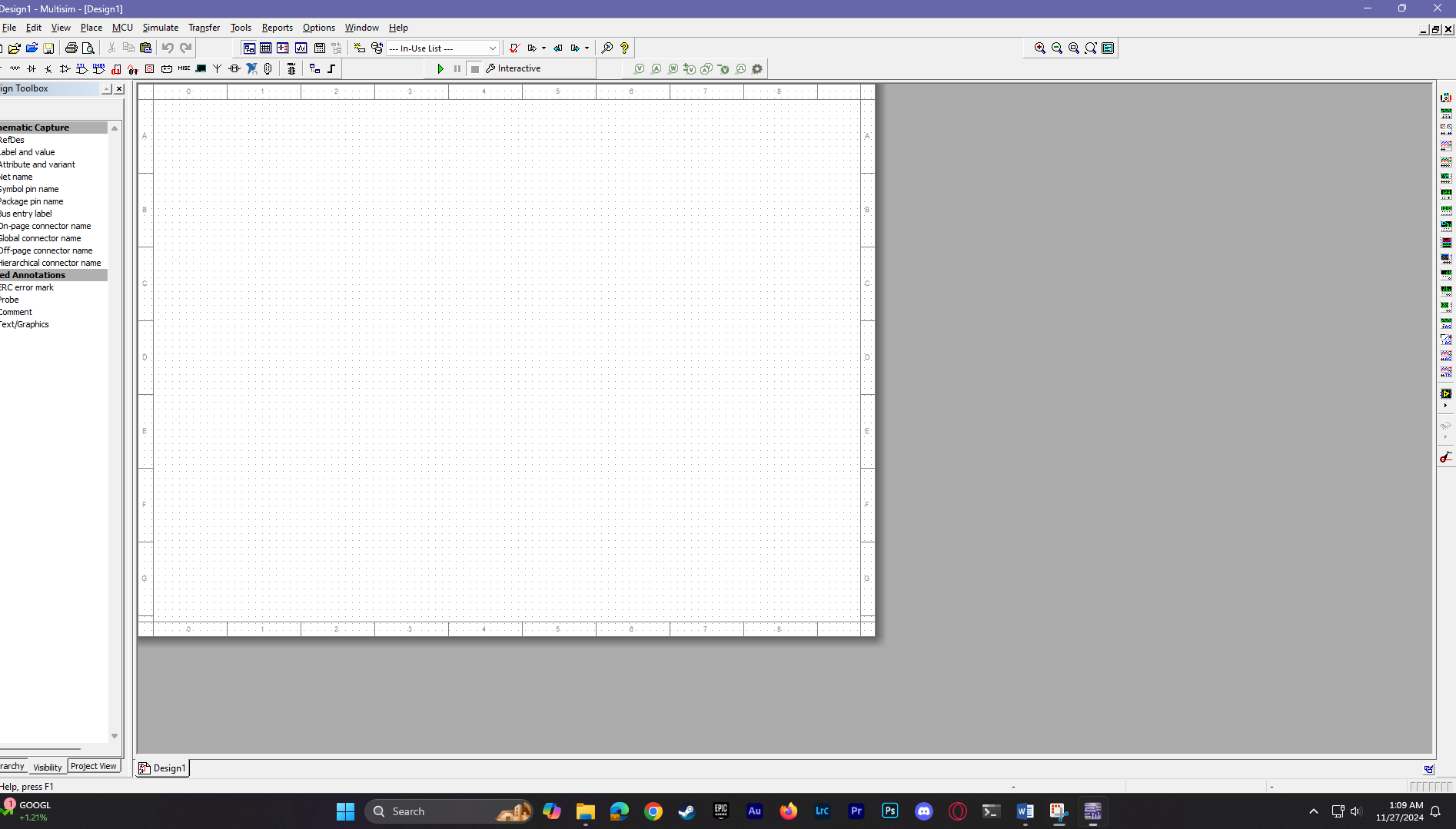
**Simulation:**

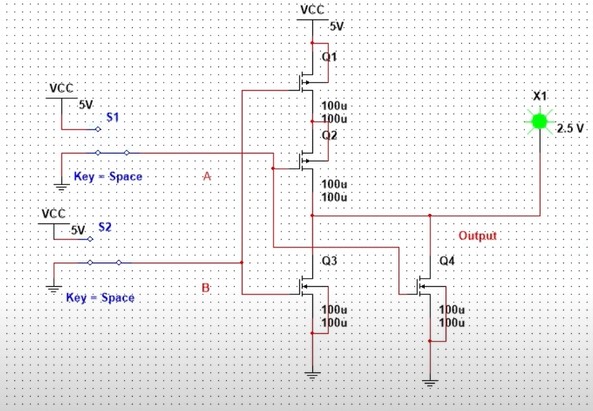




**3-input ECL NOR GATE:**

**Figure:** **3-input ECL NOR gate**

**Simulation:**



**Results and Discussions:**

In this part of the experiment, we implemented applications of AND, OR, and two-input AND-OR gates using transistors. The circuit was successfully constructed, and we achieved the expected results. Two switches were used to match the output with the truth table. However, some errors were encountered during the experiment, including instrumental errors and issues while implementing the RTL inverter. The RTL inverter experienced malfunctions that affected its performance. We used switches to toggle the input states (ON and OFF) to obtain the desired output.

TTL (Transistor-Transistor Logic) is a digital circuit technology that utilizes resistors and bipolar junction transistors (BJTs). It is called transistor-transistor logic because the transistors perform both logic gating (e.g., AND functions) and amplification. In contrast to RTL and DTL, TTL is a widely recognized integrated circuit (IC) family used in various applications such as computers, industrial controls, test equipment, consumer electronics, synthesizers, and more. Even when not directly related to TTL ICs, the term "TTL" is often used to describe TTL-compatible logic levels, such as those labeled on the inputs and outputs of electronic instruments.

Errors Faced During the Experiment:

Instrumental errors caused variations in output measurements.

The RTL inverter did not operate correctly, leading to unexpected outputs in certain cases.

Fluctuations occurred in switch-based inputs, potentially due to contact issues or improper connections.

**References:**

1. Thomas L. Floyd, *Digital Fundamentals*, 9th Edition, 2006, Prentice Hall.
2. Boylestad, Robert L., *Electronic Devices and Circuit Theory*, Pearson Education, 2009.